In re Patent Application of:
ENGLAND
Serial No. **09/825,132**
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In the Specification:

Please replace the paragraph beginning on Page 2, line 8, with the following rewritten paragraph:

For example, as shown in the reduced complexity multi-panel array configuration of Figure 1, a typical omni-directional coverage architecture places a plurality (three in the illustration) of antenna panel arrays 11, 12 and 13 in mutually orthogonal (X,Y,Z) planes, ~~21, 22 and 23,~~ to allow one or more of the panel arrays to 'see' the signal of interest, irrespective of the orientation of the antenna relative to the direction of incidence of the signal. Each panel array contains a plurality of antenna elements spatially distributed on a planar surface and electronically controlled to form a prescribed beam pattern.

Please replace the paragraph bridging Pages 11-12, beginning on Page 11, line 27, with the following rewritten paragraph:

The overall architecture of a multi-phased array antenna architecture which employs a combined baseband decision driven carrier demodulation scheme in accordance with the present invention is diagrammatically illustrated in Figure 5. The antenna itself may be comprised of a plurality of antenna panel arrays, as shown at 11, 12 and 13 in the antenna configuration of Figure 1, and mounted in mutually orthogonal (X,Y,Z) generally planar support surfaces. ~~21, 22 and 23.~~ Now although the support surfaces for antenna panel arrays 11, 12

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and 13~~, 21, 22 and 23~~ of the diagrammatic illustration of Figure 1 are in relatively close proximity (e.g., akin to three mutually adjacent sides of a 'cube', it is to be understood that such surfaces are merely illustrative and not limitative of the invention. As pointed out above, in a practical, real world environment, such as aboard a dynamic platform (e.g., ship), it can be expected that the support surfaces may be spaced apart from one another, typically at whatever locations are available. The number and orientation of panel arrays are such as to provide the intended spatial (e.g., full hemispherical) coverage. Also, as in the architecture of Figure 1, each panel array contains a plurality of spatially distributed antenna elements that are electronically controlled to form a prescribed beam pattern for that array.

Please replace the paragraph bridging Pages 12-13, beginning on Page 12, line 24, with the following rewritten paragraph:

As shown in the signal processing system diagram of Figure 5, the panel array outputs are coupled to associated LNAs 51, 52, 53, whose outputs are downconverted in respective downconverters 61, 62, 63. The IF signals produced thereby are applied to respective carrier demodulators 71, 72, 73, which are operative to regenerate a coherent carrier reference signal that is used to demodulate each respective panel's output signal. As will be described with reference to the detailed circuit diagram of Figure 6, each demodulator contains a matched filter bit detector that converts the

demodulated signal to soft bit decisions. The soft bit decisions are time aligned, weighted and subjected to an ambiguity resolution process to produce demodulated signals. These demodulated signals are coupled to and summed together in a diversity combiner 80, which outputs ~~produce~~ a composite-based bit decision to a baseband signal processor in the form of a bit synchronizer 90 for clock regeneration and data recovery. The output of the bit synchronizer 90 is supplied to the user for subsequent processing.

Please replace the paragraph beginning on Page 3, line 8, with the following rewritten paragraph:

The output of the phase detector 115 is coupled to an associated weighting circuit 123, wherein it is weighted in accordance with the external control signal from the system microcontroller (not shown) according to its relative signal-to-noise ratio, as described above. The weighted phase detector outputs of the quadrature demodulators are combined in summing circuit 77 to provide a composite phase error voltage. This ~~phase~~ composite phase error voltage is filtered in an automatic frequency control (AFC) loop filter 79 and applied to the frequency synthesizer 84 that generates the secondary IF signals to the carrier demodulators, as described above.